WHAT IS CLAIMED IS:

1. A semiconductor memory device having a data latch circuit, the semiconductor memory device comprising:

a plurality of bit lines to which a reprogrammable memory cell is connected;

a data bus on which data is transferred;

a latch connected to each of the plurality of bit lines;

a read out circuit connected to the data bus; and

a data transfer circuit group having an ability to directly transfer the data loaded in the latch circuit, to the read out circuit without being transferred to the memory cell.

2. The semiconductor memory device of Claim 1, wherein the data transfer circuit group includes:

a first operation mode to transfer a data loaded to the latch circuit, to the memory cell connected to the bit line;

a second operation mode to transfer the data read out from the memory cell to the read out circuit; and

a third operation mode to directly transfer the data loaded in the latch circuit, to the read out circuit.

3. The semiconductor memory device of Claim 2, wherein:

the third operation mode is performed during a test of the semiconductor memory device.

4. The semiconductor memory device of Claim 2, wherein:

the first and second operation modes are performed during a normal operation; and

the third operation mode is performed during a test of the semiconductor memory device.

5. The semiconductor memory device of Claim 1, wherein the data transfer circuit group includes:

a first transfer gate, one end of which is electrically connected to the bit line;

a second transfer gate, one end of which is electrically connected to an other end of the first transfer gate;

a third transfer gate, one end of which is electrically connected to the one end of the first transfer gate and an other end of which is electrically connected to the latch circuit; and

a fourth transfer gate, one end of which is electrically connected to an other end of the second transfer gate and an other end of which is electrically connected to the read out circuit.

6. The semiconductor memory device of Claim 5, wherein:

when data loaded to the latch circuit is transferred to the memory cell, the first transfer gate is set to an ON state, the second transfer gate is set to an OFF state, the third transfer gate is set to an ON state, the fourth transfer gate is set to an OFF state;

when the data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to an ON state, the second transfer gate is set to an ON state, the third transfer gate is set to an OFF state, the fourth transfer gate is set to an ON state;

when the data loaded to the latch circuit is directly transferred to the read out circuit not via the memory cell, the first transfer gate is set to an OFF state, the second transfer gate is set to an ON state, the third transfer gate is set to an ON state, the fourth transfer gate is set to an ON state.

7. The semiconductor memory device of Claim 6, wherein:

a potential of the control electrode of the third transfer gate is gradually raised to an ON state.

8. The semiconductor memory device of Claim 5, wherein:

when the data loaded to the latch circuit is transferred to the memory cell, the first transfer gate is set to an ON state, the second transfer gate is set to an OFF state, the third transfer gate is set to an ON state, the fourth transfer gate is set to an OFF state;

when the data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to an ON state, the second transfer gate is set to an ON state, the third transfer gate is set to an OFF state, the fourth transfer gate is set to an ON state;

when the data loaded to the latch circuit is transferred to the read out circuit, the first to the fourth transfer gates are set to an ON state, and the memory cell is set to a non-selected state.

9. The semiconductor memory device of Claim 8, wherein:

a potential of the control electrode of the third transfer gate is gradually raised to an ON state.

10. The semiconductor memory device of Claim 1, further comprising:

a control circuit configured to control the transfer gate group so as to achieve a first operation mode and a second operation mode, wherein:

the first operation mode involves programming data loaded to the latch circuit to the memory cell; and

the second operation mode involves stopping an operation after data is loaded to the latch circuit.

11. The semiconductor memory device of Claim 10, wherein:

the first operation mode is performed in a normal operation; and

the second operation mode is performed in a testing operation.

12. The semiconductor memory device of Claim 1, further comprising:

an error correction circuit that is electrically connected to the read out circuit.

13. A semiconductor memory device having a data latch circuit, the semiconductor memory device comprising:

a plurality of bit lines to which a reprogrammable memory cell is connected;

a data bus on which data is transferred;

a latch circuit configured to latch the data transferred on the data bus;

a read out circuit connected to the data bus; and

a data transfer circuit group;

wherein the data transfer circuit group is controlled so as to transfer the data latched in the latch circuit to the read out circuit without being transferred to the memory cell.

14. The semiconductor memory device of Claim 13, wherein the data transfer circuit has:

a first operation mode to transfer data loaded to the latch circuit to the memory cell connected to the bit line;

a second operation mode to transfer data read out from the memory cell to the read circuit; and

a third operation mode to directly transfer the data latched in the latch circuit to the read circuit.

15. The semiconductor memory device of Claim 14, wherein:

the third operation mode is performed during a test of the semiconductor memory device.

16. The semiconductor memory device of Claim 14, wherein:

the first and the second operation modes are performed during a normal operation; and

the third operation mode is performed during a test of the semiconductor memory device.

17. The semiconductor memory device of Claim 13, wherein the data transfer circuit group includes:

a first transfer gate, one end of which electrically connected to the bit line;

a second transfer gate, one end of which electrically connected to an other end of the first transfer gate;

a third transfer gate, one end of which electrically connected to the one end of the first transfer gate and an other end of which electrically connected to the latch circuit; and

a fourth transfer gate, one end of which electrically connected to an other end of the second transfer gate and an other end of which electrically connected to the read out circuit.

18. The semiconductor memory device of Claim 17, wherein:

when data loaded in the latch circuit is transferred to the memory cell, the first transfer gate is set to an ON state, the second transfer gate is set to an OFF state, the third transfer gate is set to an ON state, the fourth transfer gate is set to an ON state;

when data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to an ON state, the second transfer gate is set to an ON state, the third transfer gate is set to an OFF state, and the fourth transfer gate is set to and ON state;

when data loaded to the latch circuit is directly transferred to the read out circuit not via the memory cell, the first transfer gate is set to an OFF state, the second transfer gate is set to an ON state, the third transfer gate is set to an ON state, the fourth transfer gate is set to an ON state.

19. The semiconductor memory device of Claim 18, wherein:

a voltage of a gate electrode of the third transfer gate is gradually raised to an ON state.

20. The semiconductor memory device of Claim 17, wherein:

when data loaded to the latch circuit is transferred to the memory cell, the first transfer gate is set to an ON state, the second transfer gate is set to an OFF state, the third transfer gate is set to an ON state, and the fourth transfer gate is set to an OFF state;

when data read out from the memory cell is transferred to the read out circuit, the first transfer gate is set to an ON state, the second transfer gate is set to an ON state, the third transfer gate is set to an OFF state, and the fourth transfer gate is set to an ON state;

when data loaded to the latch circuit is transferred to the read out circuit, the first to the fourth transfer gates are set to an ON state, and the memory cell is set to a non-selected state.

21. The semiconductor memory device of Claim 20, wherein:

a voltage of a gate electrode of the third transfer gate is gradually raised to set to an ON state.

22. The semiconductor memory device of Claim 13, further comprising:

a control circuit configured to control the transfer gate group so as to achieve a first and second operation modes, wherein:

the first operation mode involves programming data loaded to the latch circuit to the memory cell; and

the second operation mode involves stopping an operation after data is loaded to the latch circuit.

23. The semiconductor memory device of Claim 21, wherein:

the first operation mode is performed in a normal operation; and

the second operation mode is performed in a testing operation.

24. The semiconductor memory device of Claim 13, further comprising:

an error correction circuit that is electrically connected to the read out circuit.

25. A test method of a semiconductor memory device, the method comprising:

latching data in a page latch via a data bus on which the data are transferred; and

transferring the data latched in the page latch to a cell matrix for storing the data in a first mode and to a read-out circuit in a second mode for testing whether or not an error occurs in a data transfer circuit group including the data bus, the page latch and read out circuit.

26. A memory card including the semiconductor memory device of Claim 1.

27. A card holder into which the memory card of Claim 26 is inserted.

28. A connecting device into which the memory card of Claim 26 is inserted.

29. The connecting device according to Claim 28, wherein:

the connecting device is connected to a computer.

30. A memory card comprising:

the semiconductor memory device of Claim 1; and

a controller that controls the semiconductor memory device.

31. A card holder into which the memory card of Claim 30 is inserted.

32. A connecting device into which the memory card of Claim 30 is inserted.

33. The connecting device according to the Claim 32, wherein:

the connecting device is connected to a computer.

34. A memory card including the semiconductor memory device of Claim 13.

35. A card holder into which the memory card of Claim 34 is inserted.

36. A connecting device into which the memory card of Claim 34 is inserted.

37. The connecting device of Claim 36, wherein:

the connecting device is connected to a computer.

38. A memory card comprising:

the semiconductor memory device of Claim 13; and

a controller that controls the semiconductor memory device.

39. A card holder into which the memory card of Claim 38 is inserted.

40. A connecting device into which the memory card of Claim 38 is inserted.

41. The connecting device of Claim 40, wherein:

the connecting device is connected to a computer.